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LPVLSI Design - A Leakage Reduction Method for Portable Devices Applications: A Review

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Abstract: In our daily life, miniaturised and compact electronic devices are integral components. All devices need charging some amount of time. In discharging time, devices are in inactive state. Why electronic devices are become battery discharge ? Because of leakage current. Transistor size becomes smaller and smaller and also it becomes faster and faster because of high density and threshold voltage falls i.e.., leakage of current. As considered scaling of VLSI geometries, consumption of static power is more influencing than others. In the VLSI, demanding of scaling and static power. Designers using stacked sleep transistor without penalization in power setup, delay and performance in circuit.

Keywords: VLSI (very large scale integration), CMOS (complementary metal oxide semiconductor),sleep transistor, cadence virtuoso.

I. INTRODUCTION

Power dissipation provided as a critical manner in the CMOS VLSI circuit, Mainly in VLSI the principle of dynamic, short circuit and leakage power are illustrated with the decreasing the low power components. For reducing the power considered two main factors are area and speed. As the consequence, the design of an able to integrated circuit in status of power, area and speed as the same instant, it is become very difficult problem.

All portable electronic devices such as wireless applications contingent on the power dissipation as the most important factor for the reason of increasing rate of battery technology.

Implementation of low power circuit is a very important thought in present semiconductor technology. Today's portable electronic device has become to gain with effort better performance. Before designing engineers were give importance towards to performance and solidness of a design and give importance to design cost. As technology improving, engineers were more convergent on to bringing high speed circuits by minify the delay. As a year's across, IC'S become a very smaller, faster and usage of power consumption in many VLSI approaches but some changes in parameter values as well as process variations. In vey large scale integration, circuit designs are trade between power, area & performance.

Low power design parameters of the below issues:

Source of power dissipation:

$$P = P_{switching} + P_{short\ circuit} + P_{leakage} + P_{static}$$

In this design, static power consumption is more dominant to reduce power dissipation in sleep transistor.
Where,

$$P = I_{static} \cdot v$$

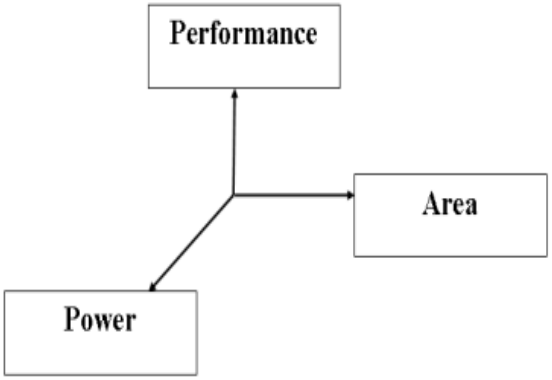

Fig.1 Parameters of VLSI

The concept of the sleep transistor is straight forward, optimal sleep transistor design and implementation are a challenge due to various effects, introduced by the sleep transistor and its implementations, on design performance, area, routability, overall power dissipation, and signal/power integrity. Optimal sleep transistor design also depends on design specific goals and chosen CMOS technology and process. A number of decisions need to be made including the choice of header or footer switch, normal or reverse body bias, optimal transistor size, and layout implementation details such as single or double row and extra rail or direct via-pillar for permanent power connection

Sub threshold leakage current (power) is becoming the primary source of power dissipation is CMOS. At smaller geometries, management of leakage current can greatly impact design and implementation choice. Till now, primary concerned were improving the performance of design and reducing silicon area to lower the cost. Now power is replacing performance as the key metric for VLSI design.

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A.SLEEP TRANSISTOR DESIGN CONSIDERATIONS :

The sleep transistor implementation introduces extra cost in chip area, routing resource, IR-drop and design complexity. There are also extra power dissipations from sleep transistors, power-gating control logic and power-on/off introduced operations. It is essential to ensure that the leakage reduction from the power gating implementation overwhelms those introduced costs to be worth the effort. To that end, various design considerations and tradeoffs need to be analyzed and handled correctly in the sleep transistor design and implementations. A good sleep transistor design is achieved by optimizing gate length and width, finger size and body-bias based on overall considerations of power efficiency, leakage current, IR-drop, area efficiency and layout impact.

B. Sleep Transistor Design Metrics :

Quality of a sleep transistor design is often measured in terms of three metrics: switch efficiency, area efficiency and IR drop. The sleep transistor is optimized in gate length, width, finger size and body-bias to achieve high switch and area efficiencies, and low leakage current and IR drop.

C. Conventional Basic CMOS approach :

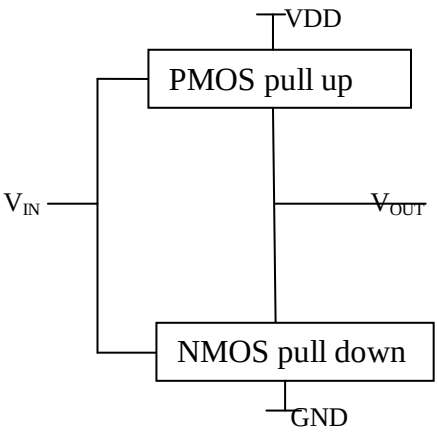

Fig.2 Basic CMOS

Above fig.2 shows the block diagram of digital circuit using conventional CMOS techniques. In this technique, a fully complementary CMOS circuit has an NMOS pull down network to connect the output to '0' (GND) and PMOS pull up network to connect the output to '1' (VDD). In this, output Get dissipated in some time. So, avid this sleep transistor are added the above circuit as shown in below fig.3.

A sleep transistor is a circuit that performs both a PMOS or NMOS high threshold voltage transistor and it is used as a switch to turn off power supplies in standby mode as shown in below fig.3. The sleep transistor PMOS settled between

Voltage of drain to drain and the pull up network hence it is called header switch and an additional sleep NMOS transistor Settled between voltage of source to source and pull down network hence it is called footer switch. In this technique happens is State destructive (outputs are floating when in sleep mode), Need retention circuitry, May be applicable for large digital blocks, Transistors with high Vth can be used.

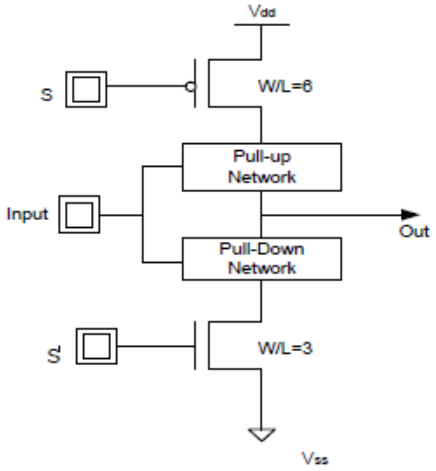

Fig.3 Sleep approach

II. LITERATURE SURVEY

Literature survey is an important part of the project. It enables assimilation of knowledge required for the project right from the problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the project.

ISSN, Vol. 1, No. 1, October 2012,IJEETC-**Anjana R1 and Ajay Kumar Somkuwar** entitled as minimizing the sub threshold leakage for high performance CMOS circuits using novel stacked sleep transistor technique - Performance characteristics such as static power dissipation, dynamic power dissipation, power, delay, power delay product was analysed for the conventional CMOS logic, stack, sleeper, sleepy stack, sleepy keeper with the proposed stacked sleep approach in 1.2 nm technology[1]. By experimental result it was found that there was 1.2 X improvement in the power dissipation with the stacked
sleeper technique.

Jun Cheol Park, Vincent J. Mooney III, and Philipp Pfeiffenberger - Sleepy Stack Reduction of Leakage Power- In this, the sleepy stack is applicable to single and multiple threshold voltages and the sleepy stack combine some of the advantages of sleep transistors – most notably the effective use of dual-*Vth* technology – with some of the advantages of the stack approach – most notably the ability to save state[2].

Se Hum Kim, Vincent J, Mooney 3 designed Sleepy Keeper : a New Approach to Low-leakage Power VLSI Design: The sleepy keeper technique results in ultra low static power consumption with state saving. Furthermore, the sleepy keeper approach is applicable to single and multiple threshold voltages. With application of dual Vth, sleepy keeper is the most efficient approach to reduce

leakage current with the smallest delay and area increases while simultaneously preserving precise logic state in sleep mode[3]. In terms of area, the sleepy keeper approach is expected to be more attractive for complex logic circuits, because the portion of increased area for the required additional transistors will be smaller for complex logic circuits than for simple logic circuits(eg., for an inverter).For our future work, we plan to investigate why the sleepy keeper approach increases dynamic power consumption over the sleepy stack approach, aiming to reduce this increase in dynamic power consumption.

International Journal of Engineering Trends and Technology (IJETT) - Volume4Issue4- April 2013 - **C.Jagadeesh, R.Nagendra, Neelima koppala** entitled as Design & Analysis of Different Types of Sleepy Methods for Future Technologies :
This paper presents a novel circuit structure named "power gated sleep method" as a new remedy for designer in terms of power products[4]. The power gated sleep method shows the least speed power product among all methods. Therefore, the power gated sleep method provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-60% of power than the existing methods. So, it can be used for future integrated circuits for power Efficiency. Advantages: State preserving, Less area overhead vs. sleep stack approach, Minimal delay. Disadvantages: Again exist in the floating of output voltage.

IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 3 - A Novel Dual Stack Sleep Technique for Reactivation Noise suppression in MTCMOS circuits **:**Designers choose techniques based upon technology and design criteria[5]. In this paper, we provide novel circuit structure named "Dual stack" as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption. Drawback of this increase in area.

International Journal of Advanced Research in Computer Science and Software Engineering - a new approach for Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS circuit for VLSI Applications **: Hina malviya, Sudha Nayar C.M Roy** RKDF Bhopal, India. RKDF Bhopal, India. MANIT Bhopal, India. In the thesis is "zigzag with keeper "and comparing the power consumption with other existing techniques[6]. The proposed technique is more effective in reducing power consumption. The result is simulated with microwind software and compare at different technology 45nm, 65nm, 90nm and 120nm.

Ultra-Low Power Designing for CMOS Sequential Circuits - **Patikineti Sreenivasulu1, Srinivasa Rao, Vinaya Babu –**
In this paper, several existing power reduction techniques are discussed and a novel circuit design technique to minimize sleep mode power consumption due to leakage power in CMOS technology is discussed. This circuit technique provides significant energy savings in sleep mode without any speed degradation or die area overhead. Moreover, it is almost independent of technology scaling and has no circuit design complexity[7].

This paper presented several dual-threshold voltage circuit techniques that can help reduce sub threshold leakage currents during standby modes for combinational logic blocks . MTCMOS was shown to be an effective standby leakage control technique for static logic, but difficult to implement since sleep transistor sizing is highly dependent on discharge patterns within the circuit block.

ISSN 2319 – 2518,Vol. 1, No. 1, October 2012 - minimizing the sub threshold leakage for high performance CMOS circuits using novel stacked sleep transistor technique, **Anjana R1 and Ajay Kumar Somkuwar** - Performance characteristics such as static power dissipation, dynamic power dissipation, power, delay, power delay product was analysed for the conventional CMOS logic, stack, sleeper, sleepy stack, sleepy keeper with the proposed stacked sleep approach in 1.2 nm technology[9].
By experimental result it was found that there was 1.2 X improvement in the power dissipation with the stacked sleeper technique.

III. APPLICATIONS

1. Intel uses "sleep transistors" to reduce power, By Jun. 14, 2002 - EE Times article revealed that Intel is planning on_using "sleep transistors" in upcoming integrated circuits. "Sleep transistors" are circuits designed to minimize power consumption and heat dissipation. Basically, the chip will contain specialized circuitry that will shut down certain areas of the chip that aren't immediately needed. The problem with this approach is that it will degrade performance somewhat, and will lead to an increased transistor count. But Intel is clearly becoming increasingly worried by heat problems, and therefore has little choice but to develop this technique.

2. Power gating is a technique used in integrated circuit (IC) design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

3. Active Leakage Control with Sleep Transistors and Body Bias - Zhengya Zhang and Zheng - In order to investigate the effectiveness of leakage power reduction, three applications were selected – a clock distribution tree, an 8-bit carry look-ahead adder, and an 8-bit address decoder – with intrinsic activity factors ranging from high to low. Each application was simulated to measure the total power dissipation before and after applying active leakage control.

IV.CONCLUSION

This paper provides a brief analysis on different approaches of sleep transistor and their performance analysis. In the proposed design a new modified stacked sleep approach will be designed for sleep transistor applications. The slep transistor will be designed using Cadence Virtuoso 6.1.1 Version, Analog Design Environment. Simulations will be carried out on different techniques to obtain the best results. Power and Delay analysis is major area of concern.

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BIOGRAPHIES

Sushma K.H was born on 14th July. She has completed his bachelor of Engineering from STJIT, Ranibennur, India. She joined M Tech VLSI with AIET, Moodbidri, India. Her major field of interest is Low power VLSI design.

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